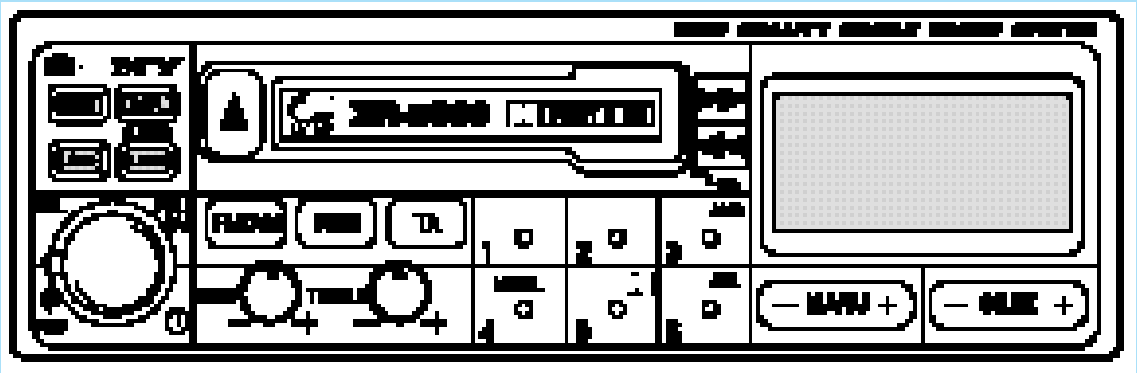
TECHNICAL INFORMATION FOR SERVICE ENGINEERS

XR-5800RDS



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1. Introduction

The SONY XR-5800RDS series are the first car radio-cassette players that include an RDS (Radio Data System) decoder. The RDS decoder features the primary RDS functions, like Programme Identification (PI), Programme Service Name (PS), Alternative Frequencies (AF) and Traffic Programme / Traffic Announcement (TP/TA). In addition, the clock time is displayed by using the CT data.

As can be seen from the simplified block diagram in figure 1.1, the set is very straightforward. It comprises an AM/FM stereo tuner with RDS decoder, an auto reverse cassette player with Dolby B Noise Reduction and a power amplifier. The differences between the related models are :

- XR-5800RDS: AM tuning range : 531 - 1602 kHz
- XR-5801RDS: AM tuning range : MW: 531 - 1602 kHz
  LW: 153 - 281 kHz
- XR-5802RDS: as XR-5800RDS but additionally with ARI decoder (current German trafic announcement system).

In the following chapters the different blocks are discussed in detail and their circuit operation is explained.

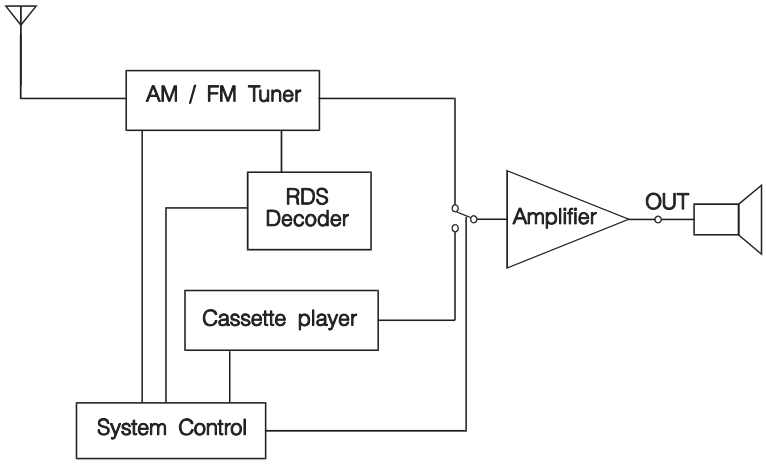

Fig. 1.1. Block Diagram of XR-5800RDS

2. Cassette player section

The cassette player circuit is shown in figure 2.1. According to the position of S902, the music signals coming from the forward or reverse heads are switched to the pre-amplifier (IC372). S902-3 informs IC701 (system controller) whether the mechanism is in the forward or reverse mode. IC372 is an OPAMP with the necessary frequency equalisation in the feedback loop. Q101, Q201 and Q301 switch the feedback loop between 120 µs (Type I-tape) and 70 µs (type II-tape and IV-tape). The L & R outputs of IC372 pass RV101 and RV201 respectively before going to the Dolby NR (IC373). RV101 and RV201 adjust the output level to ensure proper Dolby Noise Reduction.

The L & R output signals are added through R106 and R206 to form the input of the AMS IC (IC371). Q372 switches the AMS feature on or off. When during FF or REW a blank space of about 4 seconds is detected, plunger PM902 will be activated via Q371 and Q373 to release the FF or REW mode. The time constant of 4 seconds is determined by C373 and R372.

S901 is switched on when a cassette has been loaded, while S903 is on during FF or REW mode. These switches provide the syscon with information about the MD. Plunger PM901 and M901 are connected in parallel and switched on by Q451 and Q452. The plunger pulls a lever that activates a gear so that the head and pinch rollers are moved towards the tape. When the tape stops running (e.g. when the power is switched off), the head and pinch rollers will be pushed back by a spring to prevent them from touching the tape.

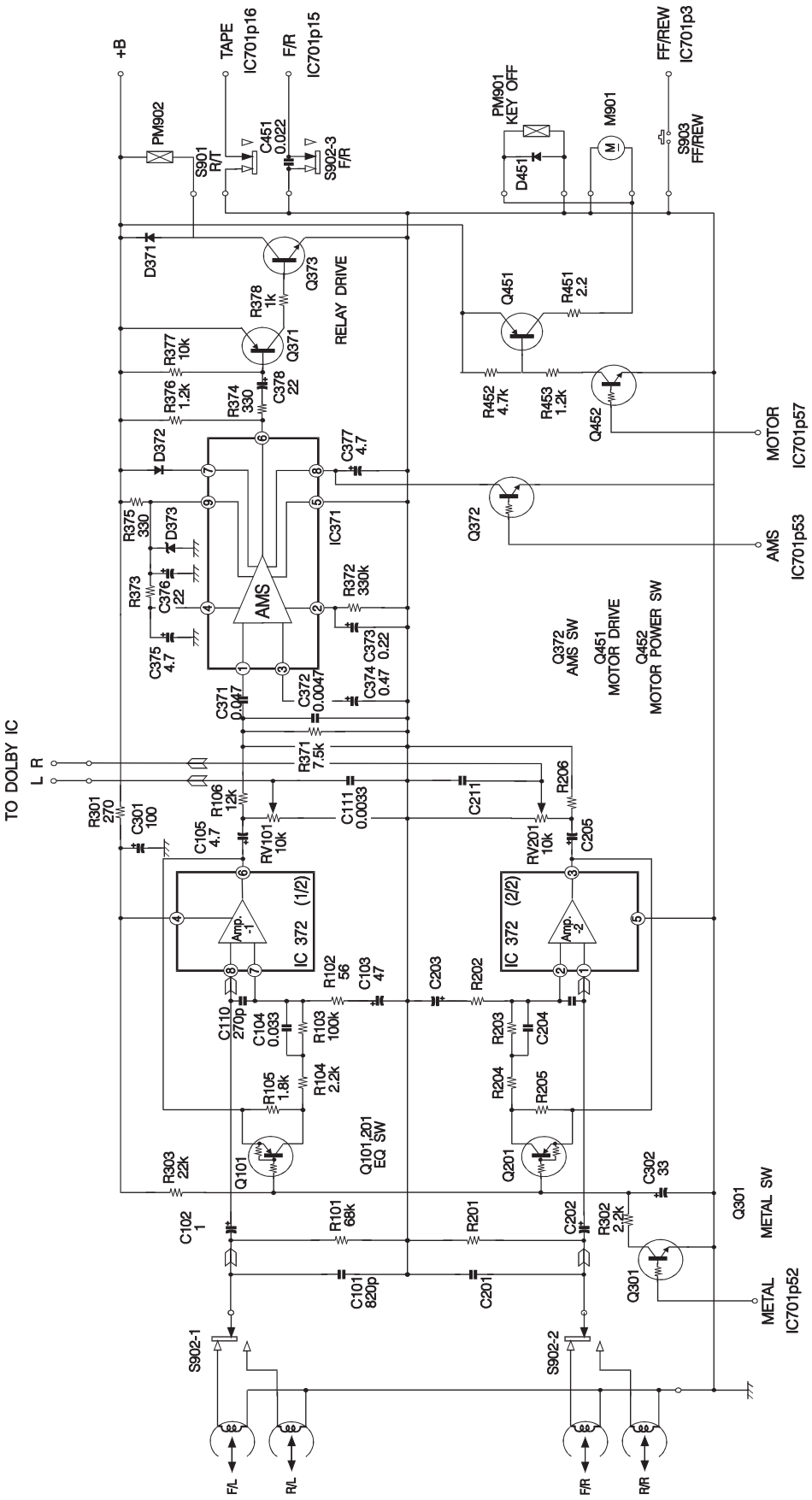

Fig. 2.1. Deck Board

3. Tuner section

3.1. AM/FM Tuner

The tuner TN1 is one single unit that contains both an AM and FM tuner with RF section, IF section and detection. This unit is almost completely controlled by the system controller (IC701). Only two adjustments can be made to the tuner unit: AM and FM Auto Scan/Stop Level adjustment.

The tuner unit is not serviceable, it should be replaced when considered defective.

3.2. FM Noise Canceller

A noise canceller is added to remove spike noises that might be generated from static discharge or by the car ignition system. The FM Noise Canceller is shown in figure 3.1.a, the block diagram of IC1 is shown in figure 3.1.b.

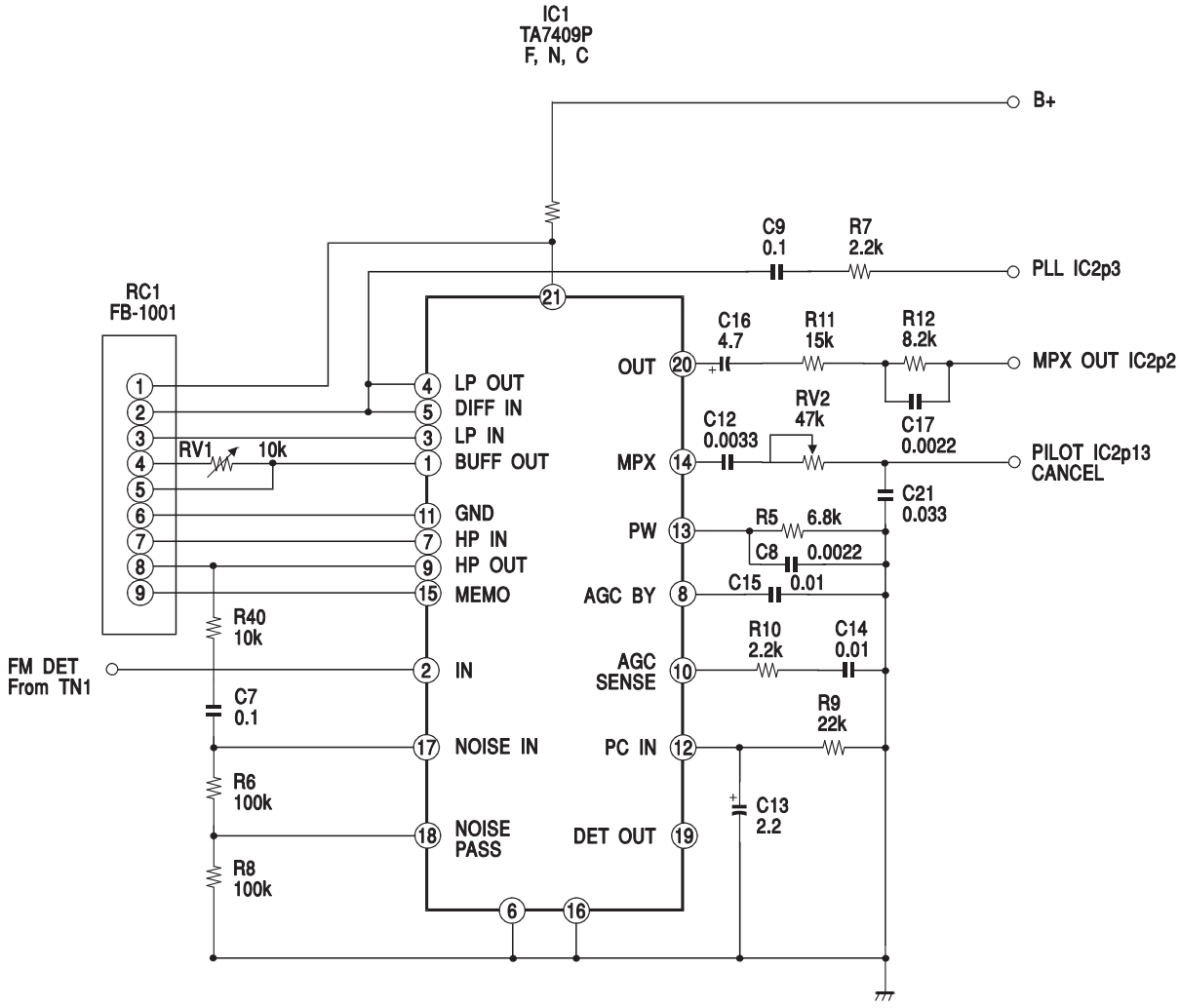

Fig. 3.1a. FM Noise Canceller

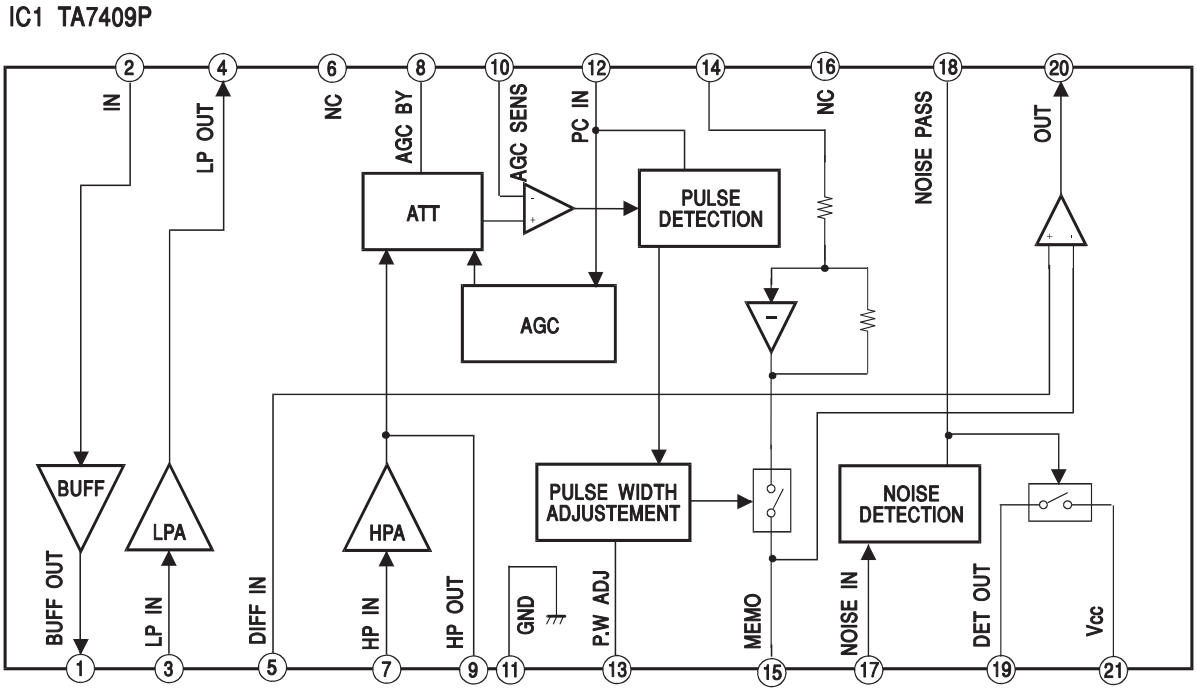

Fig. 3-1b. IC1 FM Noise Canceller

The demodulated FM MPX signal from the tuner unit is fed to pin 2 of IC1 (buffer input). The buffered signal is available at pin 1 and is split in two paths. One path going to a low pass filter, the other to a high pass filter. The RC1 network comprises both a passive LP and HP filter. Because the spike noises contain a lot of harmonic frequencies, they pass through the HP filter and get detected by the pulse noise detection circuit. Noise AGC is used so that only impulse noises are removed, the Noise Canceller has no effect on noise arising from decreased signal strength. The output of the LP filter acts as a time-delay unit. When the signal reaches the gate, the noise has been detected earlier and the gate opens so that only the LP filtered signal can pass through. R5 and C8 determine the gating time. To compensate for a sudden drop in output level when the gate opens, a memo circuit is added.

A second noise detector is included, its ouput is used to facilitate automatic tuning and is connected to the Station Detector (SD) input of IC701 (pin 28) via Q3 and Q4.

The output of the Noise Canceller (IC1, pin 20) is fed to the MPX decoder (IC2, pin 2), where Stereo decoding is performed. Its outputs are the left and right music channels which are connected to IC373 (Dolby NR IC).

3.3. RDS demodulator

Figure 3.2 shows the block diagram of the RDS demodulator and figure 3.3 the schematic diagram. The FM multiplex signal from the detector in the FM front end is fed to the stereo decoder, the ARI decoder (XR-5802 only) and the RDS demodulator.

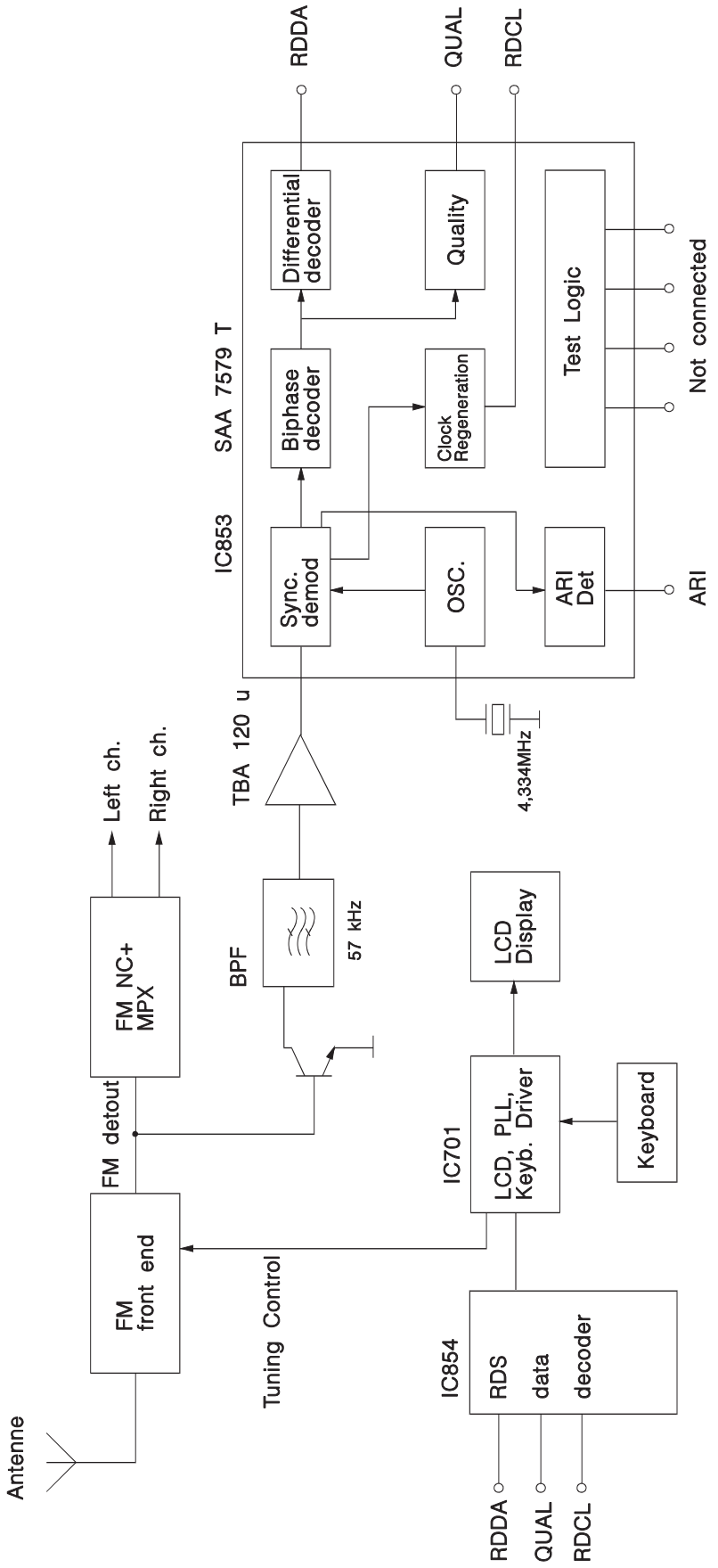

Fig. 3.2. Block Diagram of RDS Demodulator

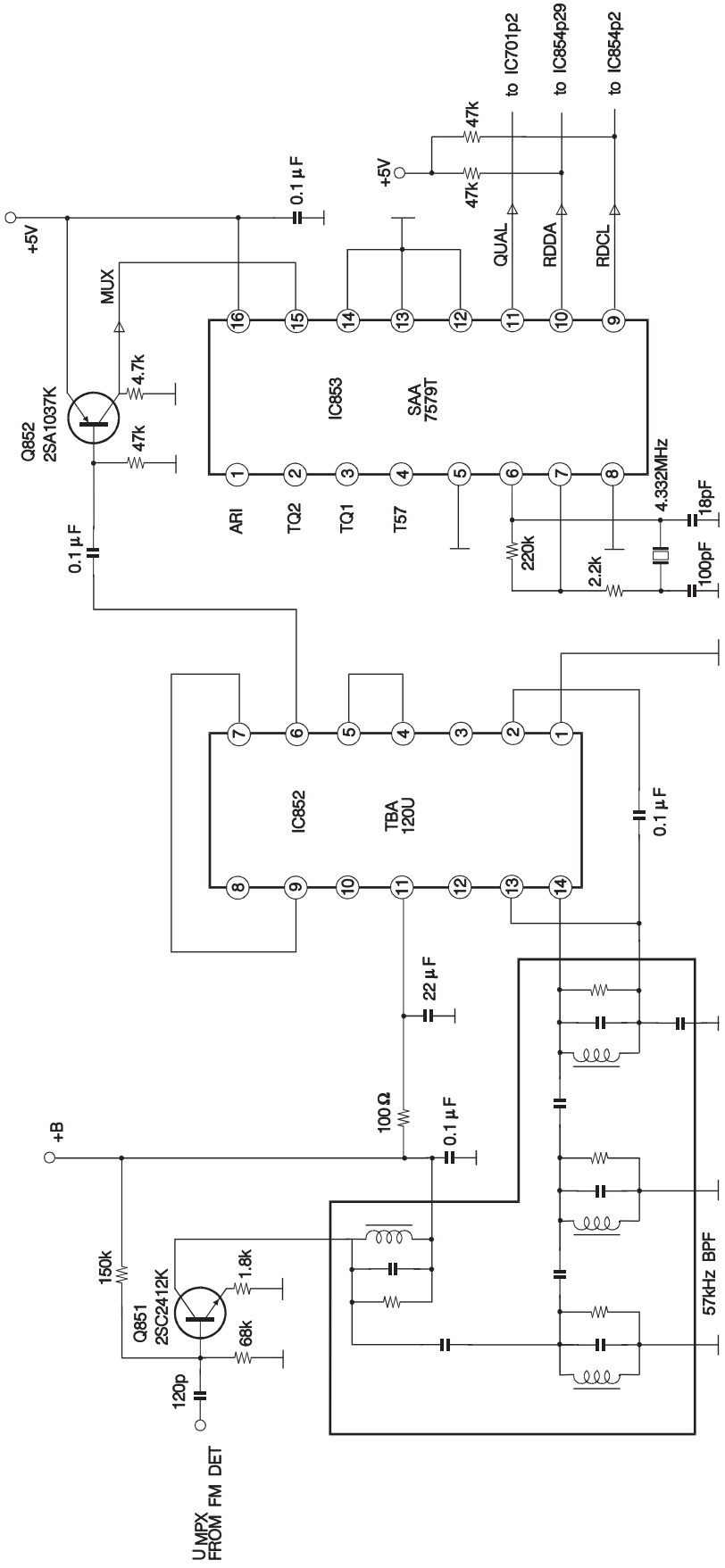

Fig. 3.3. RDS Demodulator

Figure 3.4 shows the spectrum of the FM Composite Multiplex signal, the RDS and ARI signals are located around the 57 kHz subcarrier. For RDS transmisions only, the subcarrier is supressed. In order to correctly demodulate the RDS signals, a way must be found to reconstruct the subcarrier.

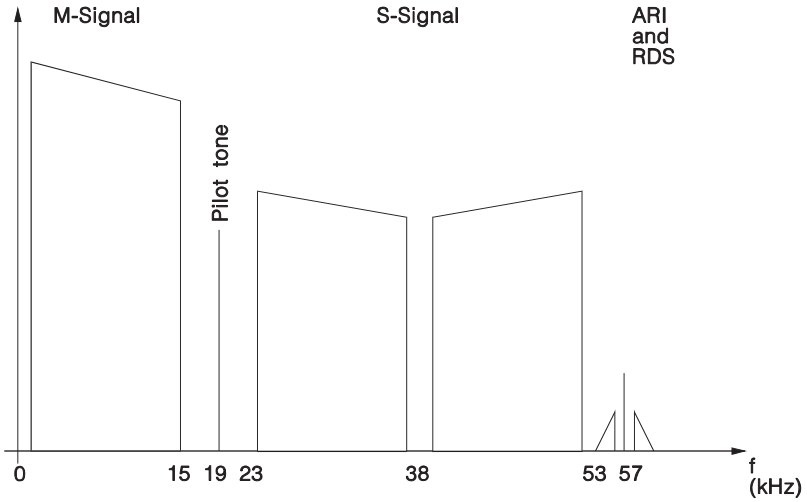

Fig. 3.4. Composite Multiplex Signal

The RDS demodulator comprises a band pass filter, an amplifier/limiter and the actual radio data demodulator, IC853 (SAA7579T). The RDS information is filtered by the 57 kHz band pass filter. This is a passive LC-filter with a bandwidth of approximately 4.8 kHz, no adjustment is necessary. IC852 (TBA120U) amplifies the signal and Q852 limits it in amplitude before feeding it to the MUX input (pin 15) of IC853.

The RDS data is AM modulated onto a 57 kHz subcarrier, because of this there are two identical sidebands. By measuring the energy in both sidebands and subtracting them from each other, an error signal is obtained. The error signal is used to control a VCO so that the synchronous demodulator stays locked on the 57 kHz. The 57kHz subcarrier frequency is derived from the master clock (X851, 4.332MHz) by dividing it by 76. The subcarrier frequency is further divided by 48 to obtain the basic clock-rate (1187.5 Hz). The Radio Data Clock (RDCL) is available at pin 9.

The demodulated Radio Data is filtered by a low pass filter (figure 3.5) before going to the biphase decoder. The biphase decoder is an integrate and dump circuit. The Radio Data now only has to be differential decoded to obtain the NRZ (Non Return to Zero) code. The demodulated Radio Data (RDDA) is available at pin 10. At pin 11 a quality bit (QUAL) is provided, this can be used to check whether the RDS data is properly demodulated (QUAL = “1" RDS data OK, QUAL = ”0" not sure about RDS data). Note that this bit has nothing to do with error checking, it only indicates that the first level of decoding the RDS data is done correctly.

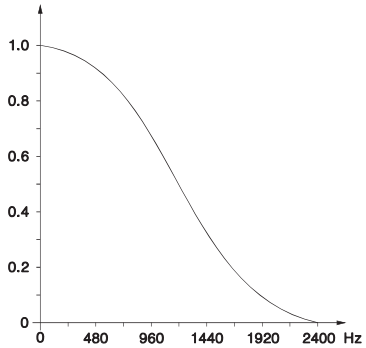

Fig. 3.5. Amplitude Response of the Data-Shaping Filter

The ARI indication at pin 1 goes HIGH when ARI signals are detected in the multiplex signal. IC853 does not decode the ARI signals, it only detects them. The ARI decoder for the XR-5802 is given in figure 3.6.

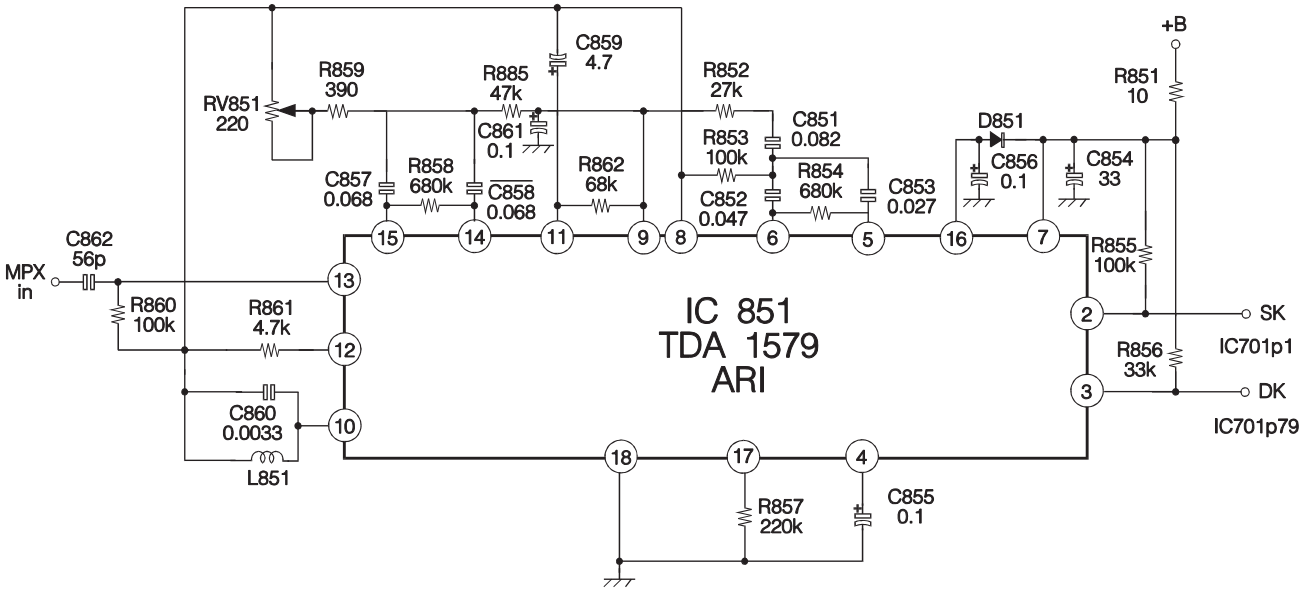

Fig. 3.6. XR5802RDS ARI Decoder

The decoding of groups and blocks, together with synchronisation and error detection and correction is done by software routines implemented in IC854. By a serial data-line the Radio Data information is passed to the system controller (IC701). It then takes appropriate action : display station name, switch to an AF, boost the volume for a TA, etc.

4. Amplifier section

The Dolby B NR circuit is shown in figure 4.1.a, figure 4.1.b shows the block diagram of IC373. IC373 is connected as a playback processor with AUX input, the AUX input being the tuner. By providing a high or low signal to pin 12, the input is respectively switched between tape PB or tuner. When in PB mode Dolby B decoding can be performed on the input signal, this is of course not possible for the AUX input. The Dolby circuit can be bypassed by supplying a high (Dolby OFF) or low (Dolby ON) signal to pin 5. These switching signals come from IC701 (Syscon). Non Dolby decoded PB signals are provided to REC OUT (pin 8, 9), in the XR-5800 they are used as test points (TP1, TP2) to adjust the Dolby NR level.

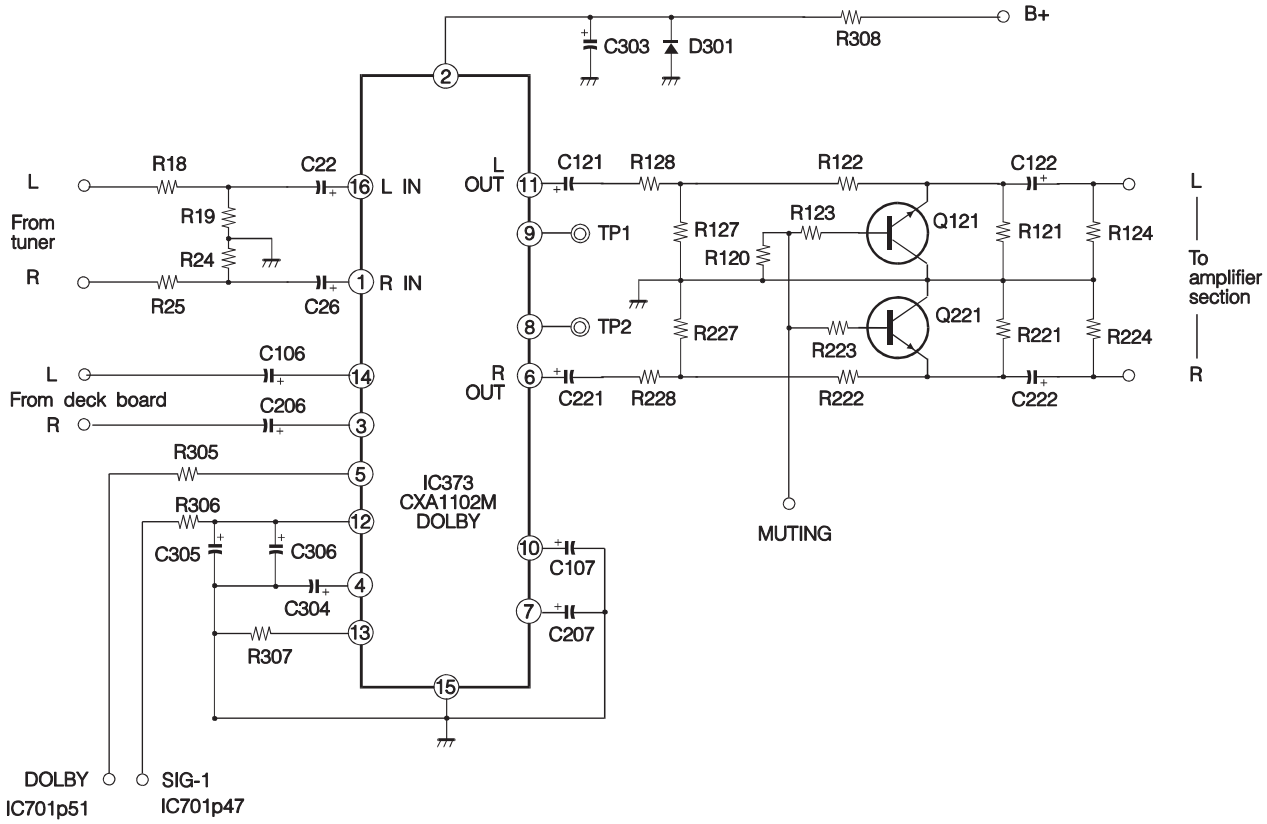

Fig. 4.1a. Dolby Noise Reduction Circuit

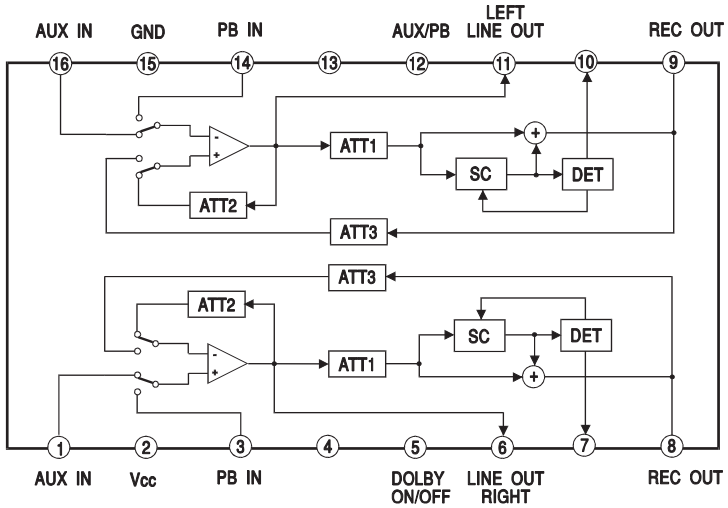

Fig. 4.1b. Dolby IC373, CXA1102M

The L & R output signals of IC373 are buffered by IC301 and followed by a common Baxandall tone control circuit (figure 4.2). The LOUD switching signal is LOW when loudness is off, so that Q321 and Q152 (Q252) are open and Q151 (Q251) is closed. When LOUD goes HIGH Q321 and Q152 (Q252) close, while Q151 (Q251) opens, this adds R154 (R254), C151 (C251) and C152 (C252) to the circuit to obtain the desired frequency response.

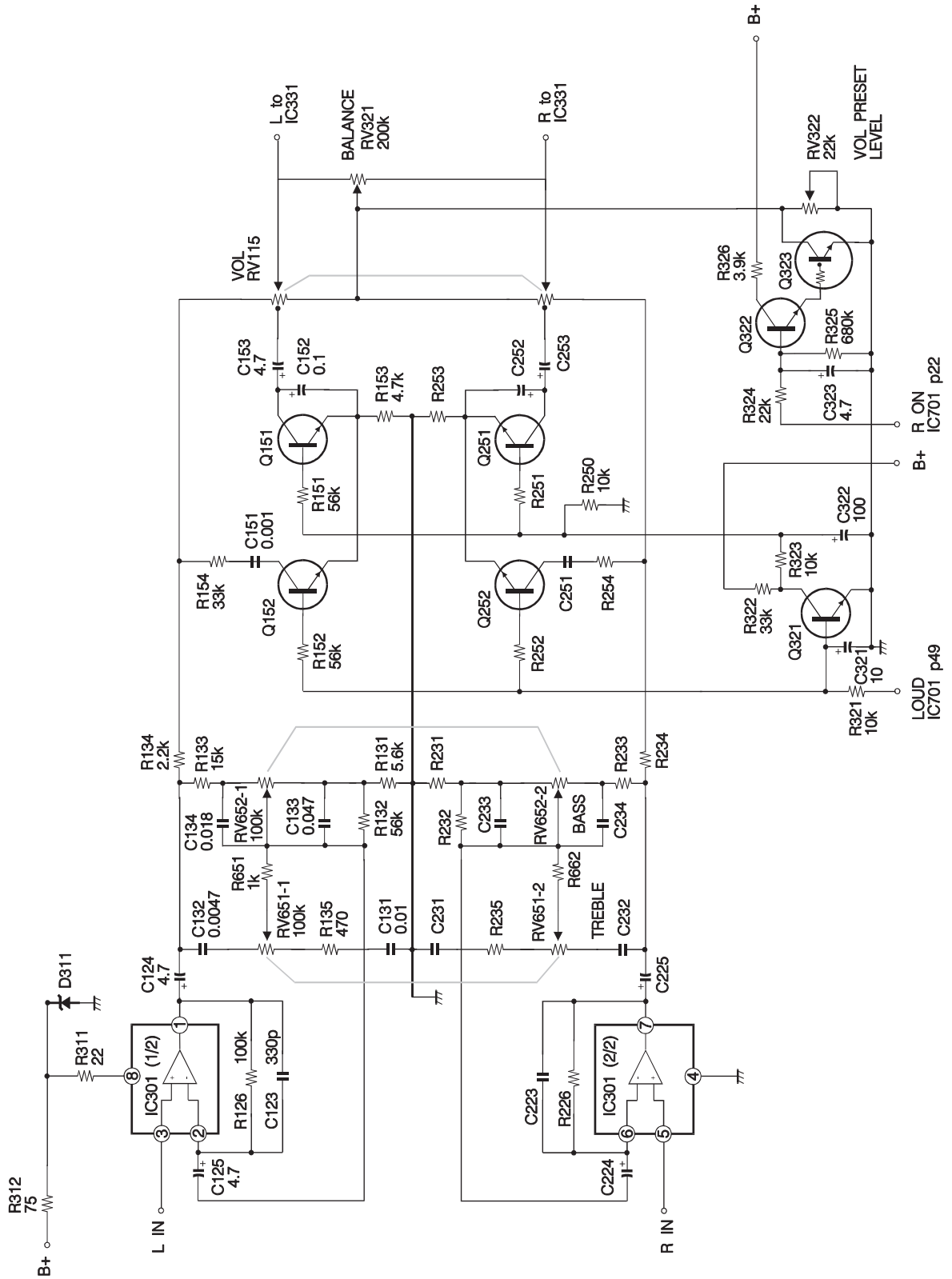

Fig. 4.2. Tone Control and Loudness Circuit

RV115 is the Volume control, note its somewhat unusual connection to obtain a Volume boost during a Traffic Announcement (TA). One side of the variable resistor is connected to ground via RV322 and Q323. During normal reception Q323 is closed, so RV115 is grounded and RV322 has no effect. When receiving a Traffic Announcement Q323 will open because of the R ON switching signal and RV115 looses its reference to ground. As a result the Volume will rise and RV115 will have only a small influence on the output level. RV322 determines the Volume Preset Level. Note that during TA RV321 (Balance control) also has no effect on the output level.

Figure 4.3 shows the line amplifier and part of the Fader circuit. Q401 and Q421 are part of the muting circuit controlled by IC701. The Fader Select switch is used to make fading possible between the line outputs and the front power outputs. This allows an external power amplifier, driving the rear speakers, to be connected to the line outputs while the built-in power amplifier drives the front speakers.

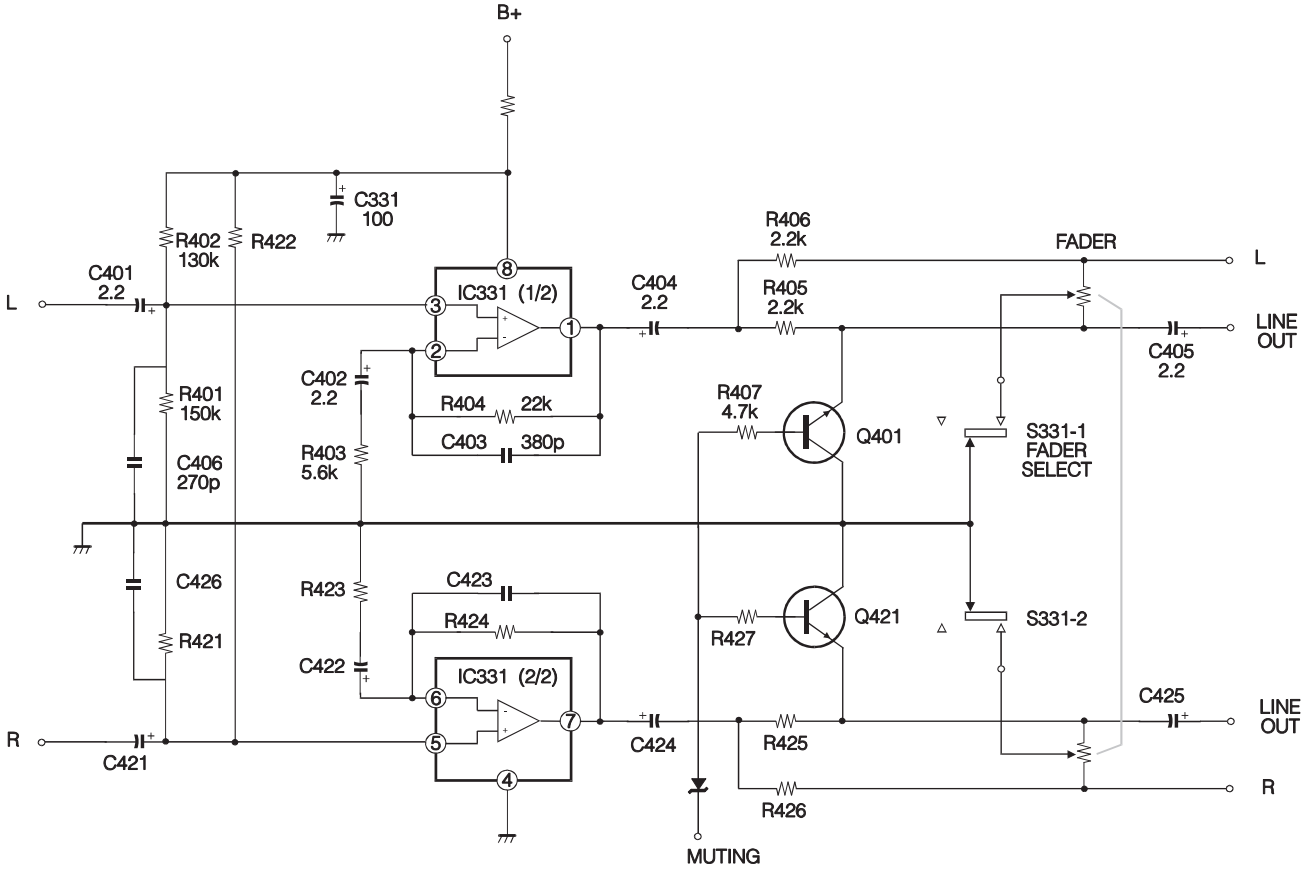

Fig. 4.3. Line Amp and Fader Circuit

The built-in power amplifier is shown in figure 4.4. It is built around IC341 (TA8221H), a power amplifier IC with overload, thermal and short circuit protection. The power supply pins (pin 10 and 17) are always connected to the accessory lead, regardless of the power supply switch. IC341 is in standby mode as long as the voltage on pin 4 is less than 2 volt. When power is switched on, the voltage on pin 4 rises to approximately 4 volt and the power amplifier switches itself on. This causes a soft start, thereby avoiding clicks in the speakers during power on. Beep pulses from IC701 are added to the music signals via the inverting inputs of the PRE-AMP. The volume setting has no effect on the level of the beeps because they are added directly to the power amplifier. The outputs of IC341 pass RV620 and RV621 (50 ohm, wirewound resistor) for Fader control before going to the speaker outputs.

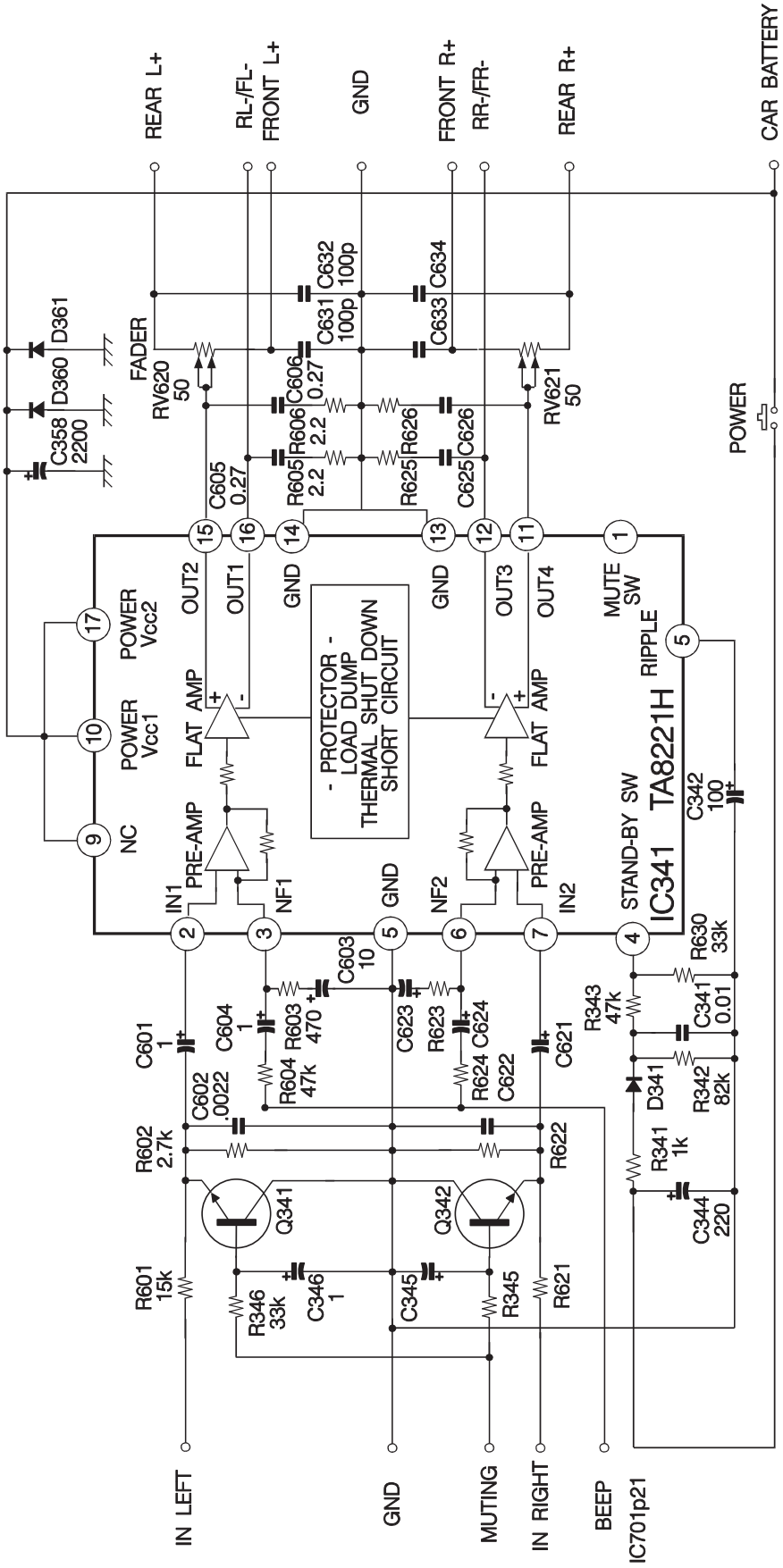

Fig. 4.4. Power Amplifier

5. Power Supply section

The BATT lead is connected to the car battery, D363 is added to prevent damage when the power supply polarity should accidently be reversed. It provides backup to IC701 for clock time (pin 12, BACKUP) and via Q706 (6V regulator) and D713 for preset memory. When this lead is not connected, e.g. when the set is taken out of its bracket, the built-in Lithium battery (BT1) provides backup via D711. However, only preset memory is retained, the clock oscillator is stopped to reduce power consumption.

The ACC lead is connected to the power switch, the power amplifier, Q361 and D357. Because of D357 the set will operate properly if only the ACC lead is connected to a power supply. When the power is switched on, the reset circuit (IC701, Q751 and Q363) will activate the muting for a brief moment. IC701 can also activate the muting (e.g. during auto tuning) via Q364.

Q355, Q356 and Q357 are parallelled to form a +9V regulator which is switched on by Q358 and Q360. It provides power to different circuits in the set, controlled by switching signals from IC701 (pin 25, AM; pin 24, FM). The deck board receives its power directly from the ACC lead via Q361. Q361 is switched on by Q362 which in turn is switched by the TAPE +B signal from IC701 (pin 50).

When a certain circuit is not working, it is a good habit to check the relevant power supply transistor and its switch-on signal because power supply problems mostly affect only part of the set.

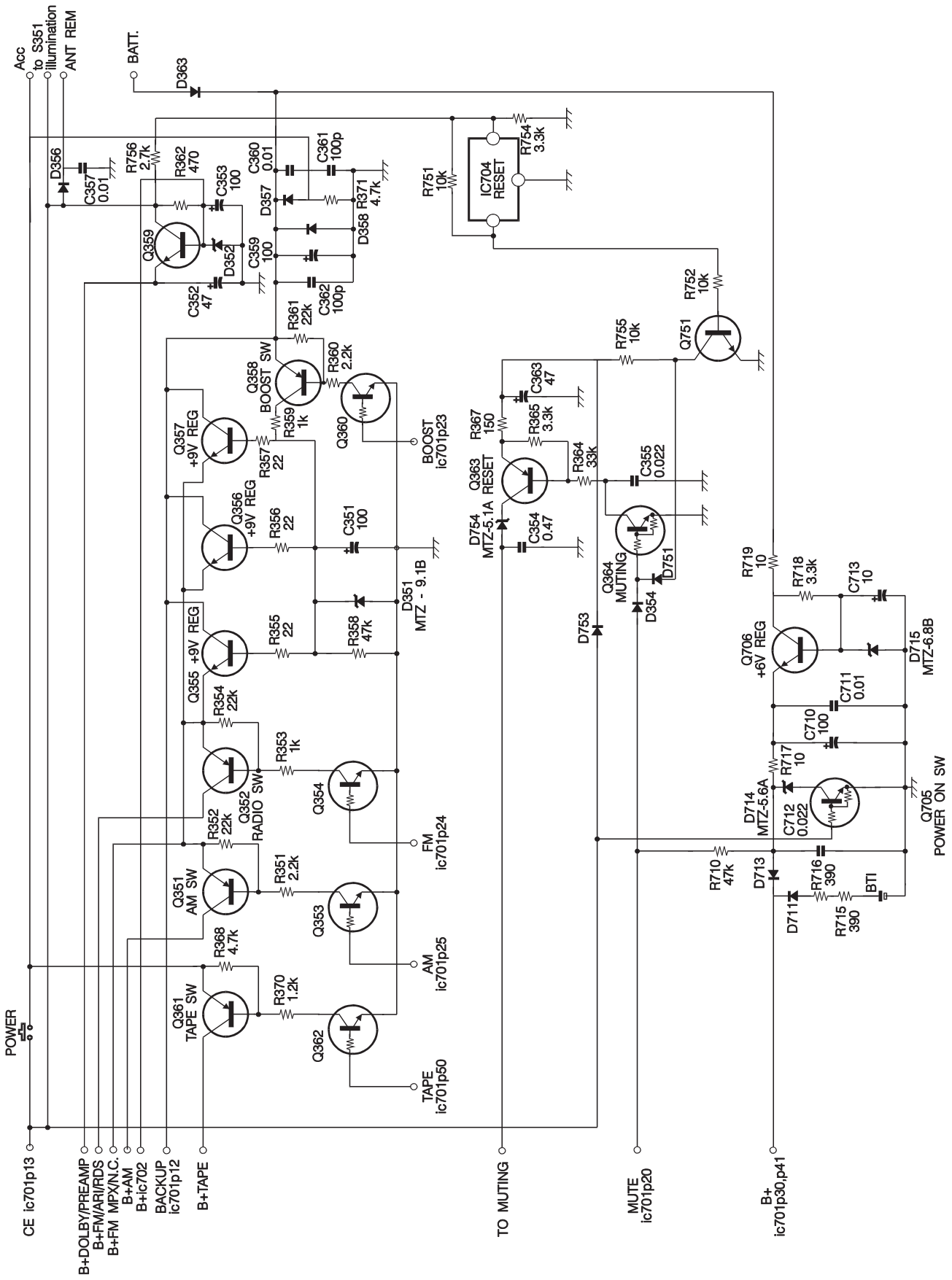

Fig. 5.1. Power Supply Section

6. System Control

IC701, µPD17003-AGF-599, is the system controller, it is an 80 pin TTL compatible CMOS device. The pin layout is shown in figure 6.1, while table 6.1 lists all pins together with their function.

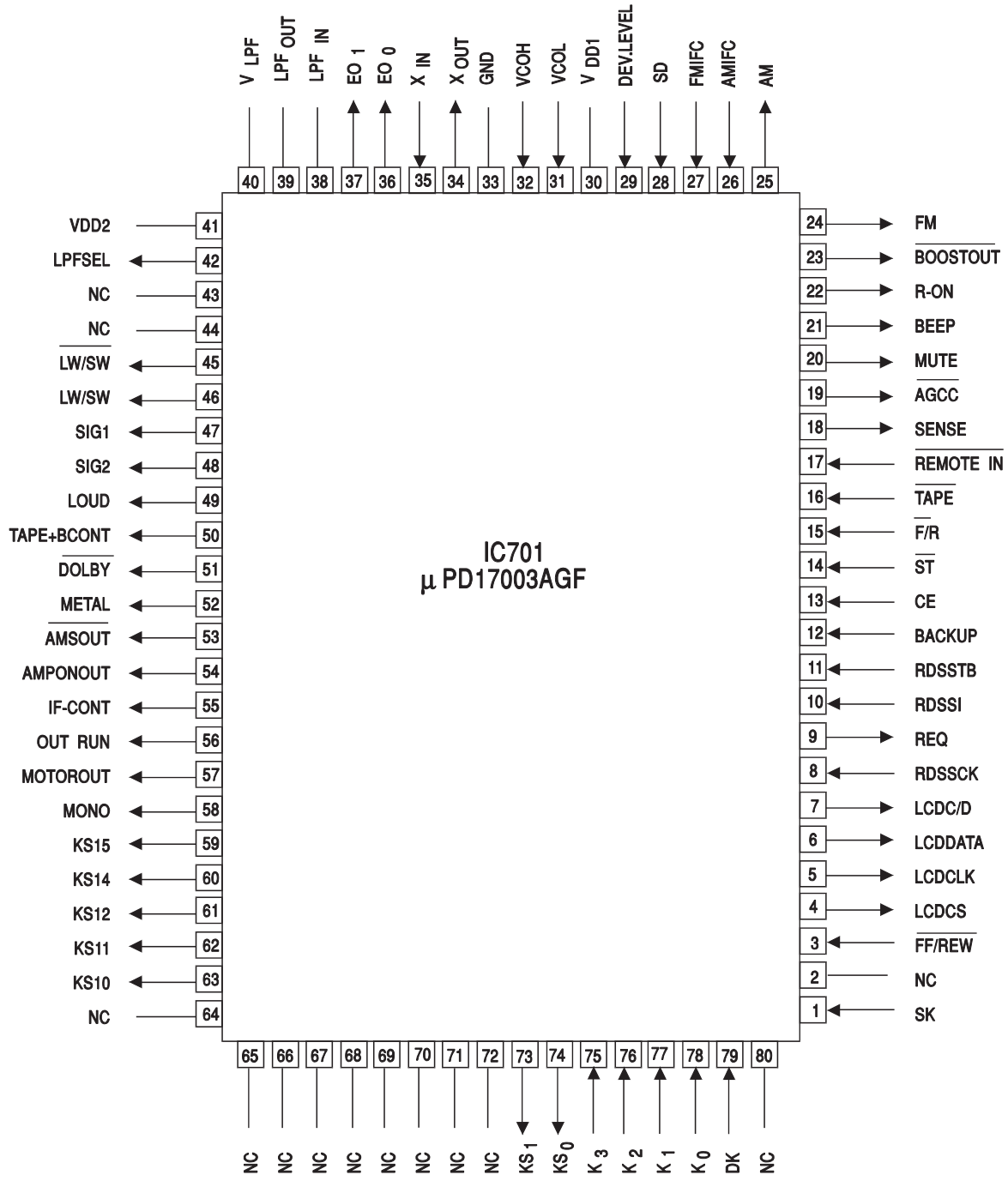

Fig. 6.1. IC701, µPD17003AGF-599 Pin Assignment

Table 6.1(a). IC701 μPD7003AGF-599 Pin Description

Pin No.	Name	I/O	Description
1	SK	I	Senderkennung (SK) ARI transmitter identification
2	RDS	I	RDS reception valid (= HIGH)
3	FF/REW	I	From S903, TAPE PB = HIGH, FF/REW = LOW
4	LCD CS	O	LCD driver enable
5	LCD CLK	O	Clock for LCD driver
6	LCD DATA	O	Serial data for LCD driver
7	LCD BLANK	O	Blank signal for LCD driver
8	RDS SCK	I	RDS Clock input
9	RDS REQ	O	RDS data request signal
10	RDS SI	I	Serial RDS data
11	RDS STB	I	RDS Strobe signal
12	BACKUP	I	Backup power input LOW in standby mode
13	CE	I	Chip enable
14	ST	I	Stereo indicator
15	F/R	I	From S902-3, FORWARD = LOW, REVERSE = HIGH
16	TAPE	I	From S901 radio/tape switch
17	REMOTE	I	not used
18	LOC	O	Local/DX
19	AGCC	O	Automatic Gain Control cut signal
20	MUTE	O	Muting control
21	BEEP	O	Buzzer output signal (2250Hz/750Hz)
22	R-ON	O	Volume preset during TA (= LOW)
23	BOOST	O	Boost signal output, LOW during TA, PTY alarm and DK
24	FM	O	FM power ON output
25	AM	O	AM power ON output
26	FM IF	I	FM IF count 10.7MHz (12.5kHz
27	AM IF	I	AM IF count 450kHz (2kHz
28	SD	I	Station Detector
29	DEV. LEVEL	I	AF switching level
30/41	Vdd	-	Positive power supply
31	AM OSC	I	AM oscillator input
32	FM OSC	I	FM oscillator input
33	GND	-	Ground potential
34/35	Xi/Xo	-	4.5MHz X-tal

Table 6.1(b). IC701 μPD7003AGF-599 Pin Description

Pin No.	Name	I/O	Description
36	EO0	O	not used
37	EO1	O	PLL error output signal
38	LPF IN	-	not used
39	LPF OUT	-	not used
40	VLPF	-	not used
42	LPF SEL	O	LPF time constant select
43/44	NC	-	not used
45	LW	O	MW = HIGH, LW = LOW
46	LW/SW	-	not used
47	SIG-1	O	Tape = HIGH, Radio = LOW
48	SIG-2	O	not used
49	LOUD	O	Loudness
50	TAPE+B	O	Deck board power
51	DOLBY	O	DOLBY OFF = HIGH, DOLBY ON = LOW
52	METAL	O	70μs switch
53	AMS	O	AMS switch
54	AMP ON	O	not used
55	IF-CONT	O	IF counter signal output
56	OUTRUN	-	not used
57	MOTOR	O	M901 ON = HIGH
58	MONO	O	Mono/Stereo selection
59~63	KS15~KS10	O	Key-return signal source
64~72	NC	-	not used
73	KS1	O	Key-return signal source
74	KS0	O	Key-return signal source
75~78	K3~K0	I	Key information input
79	DK	I	Durchsagekennung (DK) ARI announcement identification
80	NC	-	not used

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